A 800MHz to 1.066GHz All Digital Delay Locked Loop With SAR Algorithm for LPDDR3 and DDR3

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• Introduction

➢ Write operation for DDR3/LPDDR3 PHY

- ✓ Align DQ with Clock & π/2 phase shift between DQ and DQS
- ✓ Fast locking with small jitter

➢ Delay Locked Loop

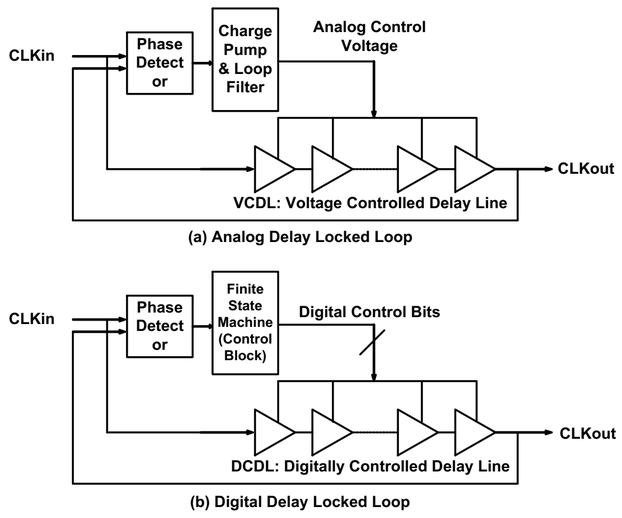


그림 1. Sort of Delay Locked Loop

• Applications

➢ Block of the proposed All Digital Delay Locked Loop

- ✓ Fast locking using inverting clock in the coarse locking process
- ✓ Coarse locking path에서 Replica Delay Line 을 제거
- ✓ Phase interpolation for possible phase shifting at fine locking process

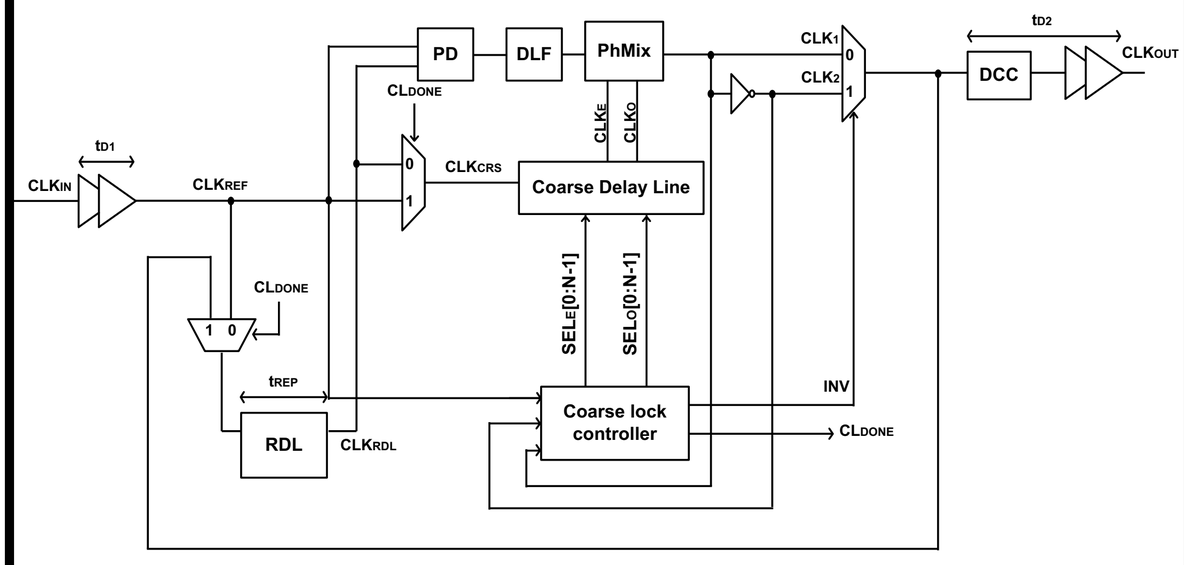
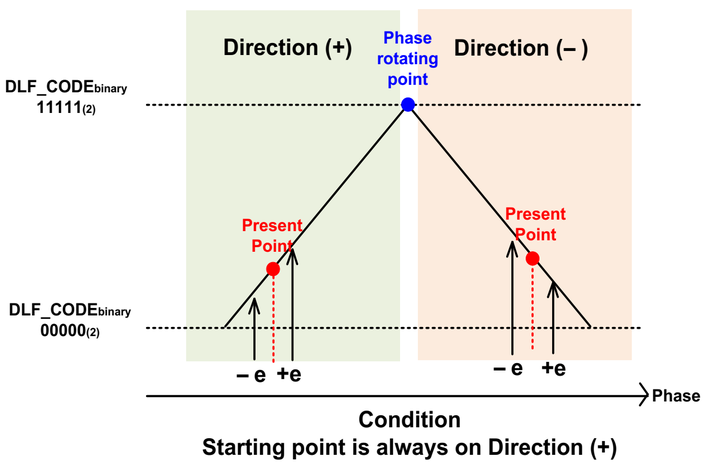


그림 2. Block of the proposed delay locked loop

➢ Bang-bang Phase detector operation

- ✓ Using Direction digital code for phase shifting
- ✓ Possible to be smooth phase shifting



Error	Direction	PD output
−e	0(+)	Late
+e	1(−)	Early
−e	0(+)	Late
+e	1(−)	Early

그림 3. Bang-bang Phase detector operation

• Bang-bang Phase Offset calibration

➢ Offset calibration application

- ✓ Phase Detector 자체 static offset 제거
- ✓ 4bit control including from -8 to 8-ps
- ✓ Calibration 동작 후 Coarse processing

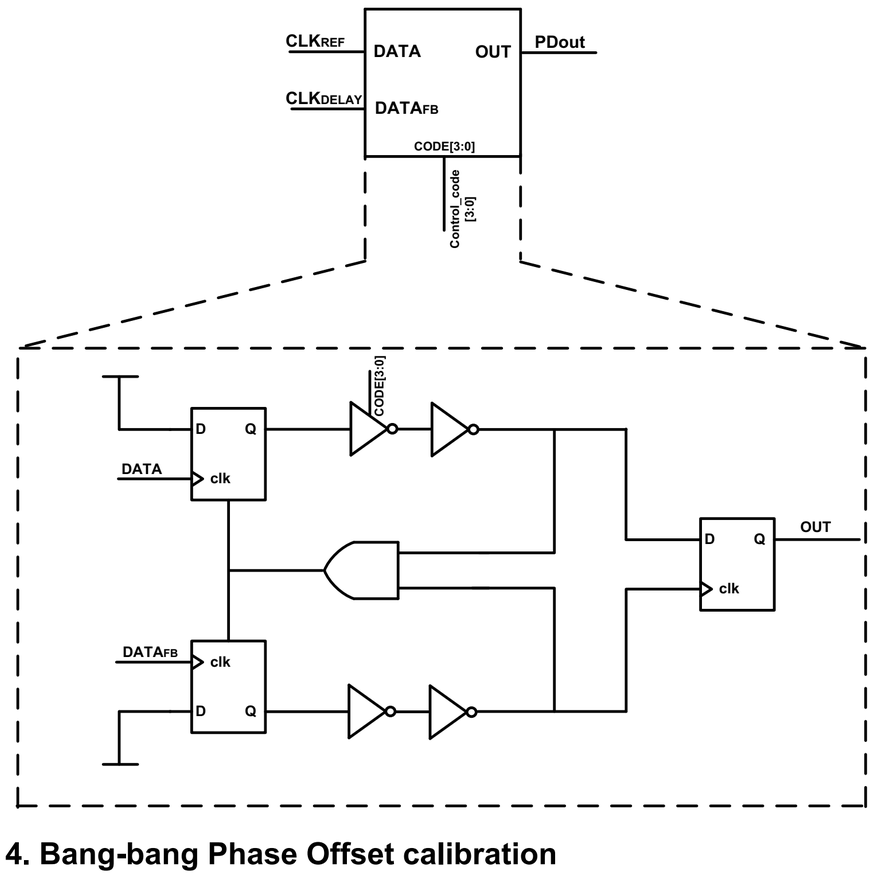


그림 4. Bang-bang Phase Offset calibration

• Simulation and Results

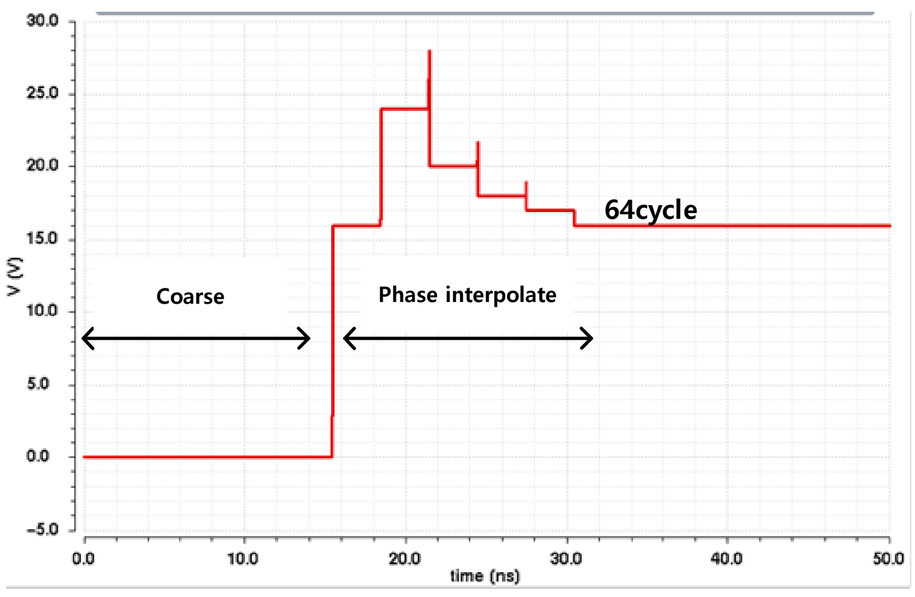


그림 5. Digtial Loop Filter Code in DLL operation

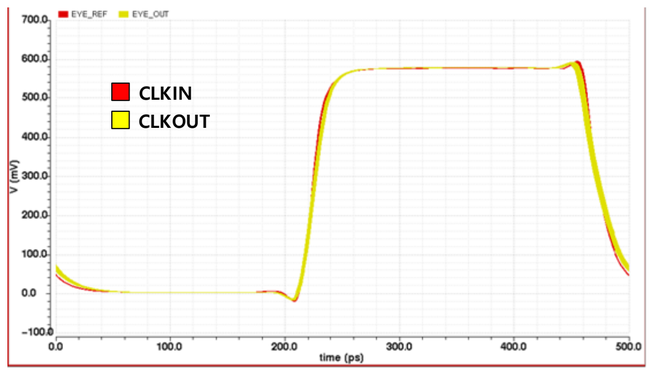


그림 6. Eye diagram for Input and Output of clock

Area	0.175-mm²
Supply	1.2-V
Power	5.7-mW
Frequency	2-GHz
jitter	1.93-ps
Locking cycle	64cycle

그림 7. Post simulation Performance Table

Acknowledgments

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