A 800MHz to 1.066GHz All Digital Delay Locked Loop With Offset Calibration Phase Detector for LPDDR3 and DDR3

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Abstract – The proposed architecture has four advantages: fast locking through SAR algorithm and fast locking through coarse locking, simplified structure for counter and offset calibration BBPD. The proposed architecture can reduce the locking cycle due to the SAR algorithm and coarse operation in the paper reported recently as a DLL applied to DDR3 and LPDDR3. In addition, it is possible to cover variation by variation, and jitter characteristic can be seen as better than conventional analog and digital architectures. This circuit type is mixed analog circuit. This project will be designed several version to achieve good performance. Therefore design size of 4mm X 4mm is needed.

I. Introduction[1]

Delay locked loop (DLL) is an important block in serial communication systems. In serial communication, the data and the clock are sent to the receiver. Here, since the characteristic of the clock varies according to the path, a DLL is used to match this. That is, DLL is a process of synchronizing a clock sent from a transmitting unit to a receiving unit in order to make a clock for receiving the data when the data comes from the transmitting unit to the receiving unit.

II. Main Body

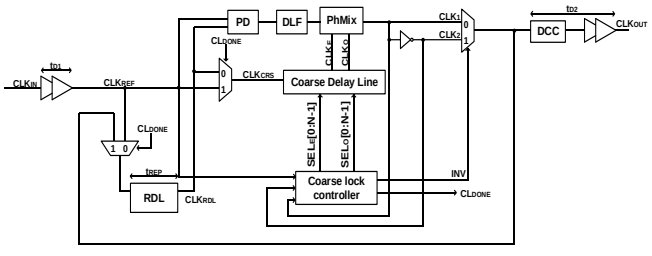
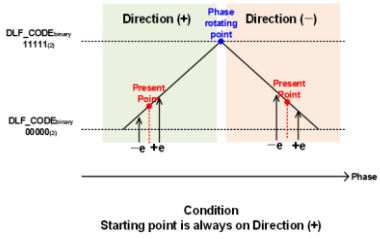


Fig. 1 Block of the proposed delay locked loop

A. Proposed Works

As shown in Fig. 1, the DLL operates with both coarse and fine measurements. Of the DLL structures, the coarse delay has proper value comparing with the resolution and cycle. The replica delay for each structure that enters each control is entered; as a solution to this, the coarse delay can reduce the feedback time without replica delays in the feedback path. Because The smaller the resolution in PI, the worse the linearity, and the larger the resolution, the larger the jitter due to BBPD, PI has 1/32 resolution of the coarse phase step in the next fine delay. In addition, it operates as a counter after initially operating with the SAR algorithm and locking in order to reduce jitter caused by the dithering caused by BBPD and latency, as well as to receive and process all the data.



Error	Direction	PD output
−e	0(+)	Late
+e	1(−)	Early
−e	0(+)	Late
+e	1(−)	Early

Fig. 2 Bang-bang Phase detector operation

The key component is Bang-bang phase detector. In Fig. 2, if there was the error in phase between reference and feedback signal, it define Early or Late that is how to adjust the phase of feedback clock. And if there was PVT variation through locking process, it has to adjust the phase in the coarse and BBPD has to adjust direction in the phase shift.

And if the BBPD has the offset, reference and output clock have little offset. That is the problem in the high speed operation. The BBPD in the proposal DLL has calibration loop to adjust the offset. It operates before the DLL operation and has two loop that the first is same input clock to the PD and the second is normally BBPD operation. The path mismatch and the mux mismatch have a little effect on

the operation in 1066MHz [1]. It adjusts its offset in the calibration operation and continues the DLL operation in Fig. 3

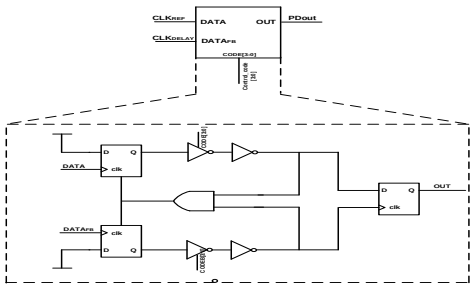


Fig. 3 Bang-bang Phase Offset calibration

III. Experimental RESULTS

The clock frequency range is 800–1066MHz, and the locking cycle proposed by LPDDR3 and DDR3 is 112 cycles.

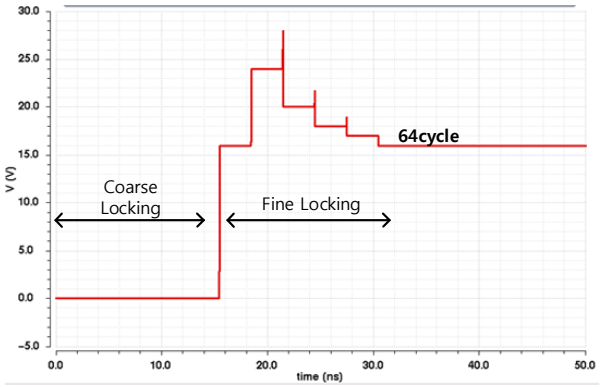


Fig. 4 Digtial Loop Filter Code in DLL operation

As shown in Fig. 4, the wake up operation and coarse locking have short time. The SAR operation in the fine locking is started in Fig. 6. If the clock reference and feedback clock is aligned, it changes the process to counter for dithering. In total, the wakeup time is short and the DLL consumes 64 cycles to lock.

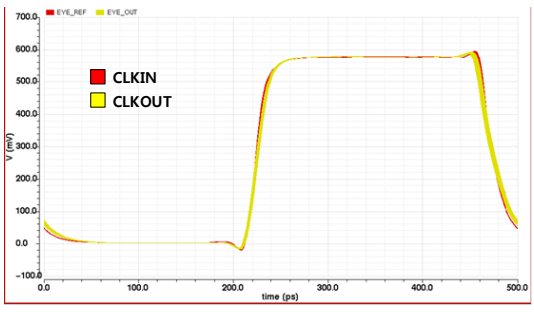


Fig. 5 Eye diagram for Clock and Output

Fig. 5, the eye diagram shows jitter performance that is measured as 1.93ps, and this jitter is the result of measuring when there is no jitter in the input clock

VII. Conclusions

The proposed architecture has four advantages: fast locking through SAR algorithm and subsampling, fast locking through coarse locking, simplified structure for counter, and SAR algorithms. The proposed architecture can reduce the locking cycle due to the SAR algorithm and coarse operation in the paper reported recently as a DLL applied to DDR3 and LPDDR3. In addition, it is possible to cover variation by variation, and jitter characteristic can be seen as better than conventional analog and digital architectures.

Acknowledgment

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References

[1] Jeffrey Prinzie and Paul Leroux, ″A Self-Calibrated Bang-Bang Phase Detector for Low-Offset Time Signal Processing,″ in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 63, NO. 5, 2016

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